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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,818	02/09/2004	Mark G. Johnson	023-0025	9232
22120	7590	05/25/2006	EXAMINER	
ZAGORIN O'BRIEN GRAHAM LLP 7600B N. CAPITAL OF TEXAS HWY. SUITE 350 AUSTIN, TX 78731			LE, THONG QUOC	
		ART UNIT	PAPER NUMBER	2827

DATE MAILED: 05/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,818	JOHNSON ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 21 March 2006.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-44 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 37-44 is/are allowed.

6) Claim(s) 1,10,13 and 24 is/are rejected.

7) Claim(s) 2-9,11,12,14-23 and 25-35 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

1. Amendment filed on 03/21/2006 has been entered.
2. Claims 1-44 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,10,13,24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hikawa et al. (U.S. Patent No. 5,666,304).

Regarding claim 1, Hikawa et al. disclose an integrated circuit (Figure 38) having two respective decode/selection circuits (Figure 38, 113,114,115,116) respectively located along opposite edges (Figure 38, 116 opposites 114, 113 opposites 115) of a three-dimensional memory array (Column 21, lines 13-30) for selecting wordlines (Column 32, lines 44-45) which respectively exit the memory array (Figure 38, MEMORY ARRAY) along the opposite edges or for selecting bitlines (Column 32, lines 44-45) which respectively exit the memory array along the opposite edges (Column 32, lines 1-47).

Regarding claim 10, Hikawa et al. disclose an integrated circuit (Figure 38) having two respective decode/selection circuits (Figure 38, 113,114,115,116) respectively located along opposite edges (Figure 38, 116 opposes 114, 113 opposes 115) of a three-dimensional memory array (Column 21, lines 13-30) for selecting wordlines (Column 32, lines 44-45) or bitlines (Column 32, lines 44-45) which respectively exit the memory array along the opposite edges (Column 32, lines 1-47), wherein the memory array comprises non-volatile memory cells (Column 1, lines 14).

Regarding claim 13, Hikawa et al. disclose a three-dimension memory array (Figure 38) having at least two planes of memory cells formed above a substrate (Figure 25, M0-M3 on substrate 71, Column 25, lines 25-27);
a first decode/selection circuit (Figure 38, 116) having outputs associated with wordlines or bitlines which exit on one edge of memory array; and
a second decode/selection circuit (Figure 38, 115) having outputs associated with wordlines or bitlines which exit on another edge opposite the one edge of memory array;

wherein the outputs of both the first and second decode/selection circuits are associated with wordlines, or the outputs of both the first and second decode/selection circuits are associated with bitlines (Column 21, lines 13-30, Column 24, lines 15-31).

Regarding claim 24, Hikawa et al. disclose wherein the memory array comprises non-volatile memory cells (Column 1, line 14).

6. Claims 1,10,13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaske et al. (U.S. Patent No. 3,696,349).

Regarding claim 1, Kaske et al. disclose an integrated circuit (Figure 11, 200) having two respective decode/selection circuits (Figure 11, 222,226,224,220) respectively located along opposite edges (Figure 11, 222 opposites 226, 224 opposites 220) of a three-dimensional memory array (Figure 11,202, ABSTRACT) for selecting wordlines (Column 9, lines 25-26, word line 14a) which respectively exit the memory array along the opposite edges or for selecting bitlines (Column 9, lines 30-31) which respectively exit the memory array along the opposite edges (Figure 1, Column 9, lines 43-46).

Regarding claim 10, Kaske et al. disclose an integrated circuit (Figure 11, 200) having two respective decode/selection circuits (Figure 11, 222,226,224,220) respectively located along opposite edges (Figure 11, 222 opposites 226, 224 opposites 220) of a three-dimensional memory array (Figure 11, 202) for selecting wordlines or bitlines (Column 9, lines 19-42) which respectively exit the memory array along the opposite edges (Figure 1), wherein the memory array comprises non-volatile memory cells (Column 9, lines 43-46).

Regarding claim 13, Hikawa et al. disclose a three-dimension memory array (Figure 11) having at least two planes of memory cells formed above a substrate (Figure 10a, 148);

a first decode/selection circuit (Figure 11, 222) having outputs associated with wordlines or bitlines which exit on one edge of memory array; and

a second decode/selection circuit (Figure 11, 220) having outputs associated with wordlines or bitlines which exit on another edge opposite the one edge of memory array;

wherein the outputs of both the first and second decode/selection circuits are associated with wordlines, or the outputs of both the first and second decode/selection circuits are associated with bitlines (Column 10, lines 5-15).

Allowable Subject Matter

7. Claims 2-9,11-12,14-23,25-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-9,11-12,14-23,25-35 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hikawa et al. (U.S. Patent No. 5,666,304), Kaske et al. (U.S. Patent No. 3,696,349), and others, does not teach the claimed invention having an integrated circuit includes half of the wordlines or bitlines respectively exit the memory array along each of opposite edges as claim 2 disclosed and decode/selection circuit are disposed in a substrate, and are folded beneath the memory array as claims 3-9, 14-23, 34-36 disclosed, and memory cell comprises passive element as claims 11,28, 30 disclosed, and anti-fuse as claims 12, 29 disclosed, a field-programmable memory cells as claim 25 disclosed, one-time-programmable memory cells as claims 26 disclosed, and memory cells which are programmable during manufacture as claim 31

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disclosed, and wherein the first and second decode/selection circuits are formed entirely in a substrate as claim 32 disclosed, and driver circuits that are formed above the substrate using materials common to the memory array as claim 33 disclosed.

8. Claims 37-44 are allowed.

Claims 37-44 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hikawa et al. (U.S. Patent No. 5,666,304), Kaske et al. (U.S. Patent No. 3,696,349), and others, does not teach the claimed invention having an integrated circuit comprising a second column selection circuit disposed at least partial beneath the memory array and having outputs along a south side of the memory array and associated with bitlines which exit the memory array to the south side thereof.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le
Primary Examiner
Art Unit 2827

5/16/2006